HI-1590

MIL-STD-1553/1760

3.3V Monolithic Dual Variable Transceiver

December 2021

DESCRIPTION

The HI-1590 is a low power CMOS dual +3.3V transceiver with the ability to vary the amplitude of the transmitter outputs. It is designed to meet the requirements of the MIL-STD-1553 / 1760 specifications, and is pin compatible to the HI-1570. The HI-1590 adds SPI communication to the onboard DAC to vary the amplitude of the transmitter outputs.

The transmitter section of each bus takes complementary CMOS / TTL Manchester II bi-phase data and converts it to differential voltages suitable for driving the bus isolation transformer. Separate transmitter inhibit control signals are provided for each transmitter. The user has the option to either supply an external voltage to a single analog input pin, or program an 8-bit DAC through a SPI port to control the transmitter output amplitude.

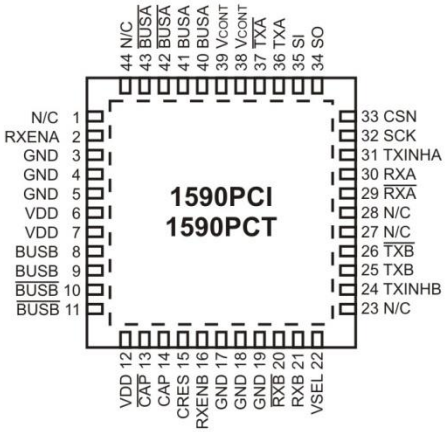
The receiver section of each bus converts the 1553 bus bi-phase differential data to complementary CMOS / TTL data suitable for inputting to a Manchester decoder. Each receiver has a separate enable input which can be used to force the output of the receiver to a logic "0".

To minimize the package size for this function, the transmitter outputs are internally connected to the receiver inputs so that only two pins are required for connection to each coupling transformer.

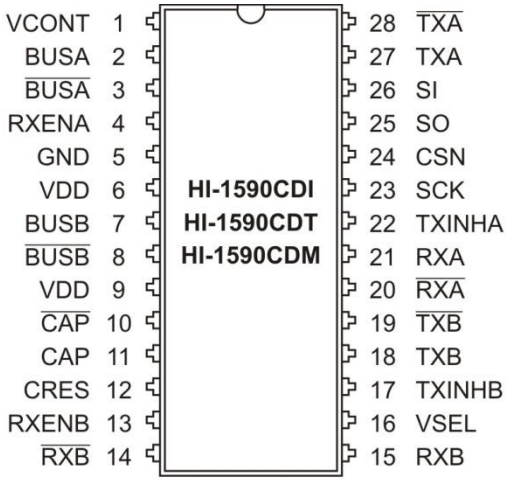
FEATURES

- Compliant to MIL-STD-1553A & B, MIL-STD-1760, ARINC 708A
- CMOS technology for low standby power
- Single +3.3V power supply
- Variable transmitter output amplitude with option to control with an external voltage or SPI controlled 8-bit DAC
- Smallest footprint available in 7mm x 7mm plastic chip-scale (QFN) package with integral heatsink
- Footprint compatible packaging options with HI-1570 or HI-1579
- Industrial and extended temperature ranges
- Industry standard pin configurations

PIN CONFIGURATIONS

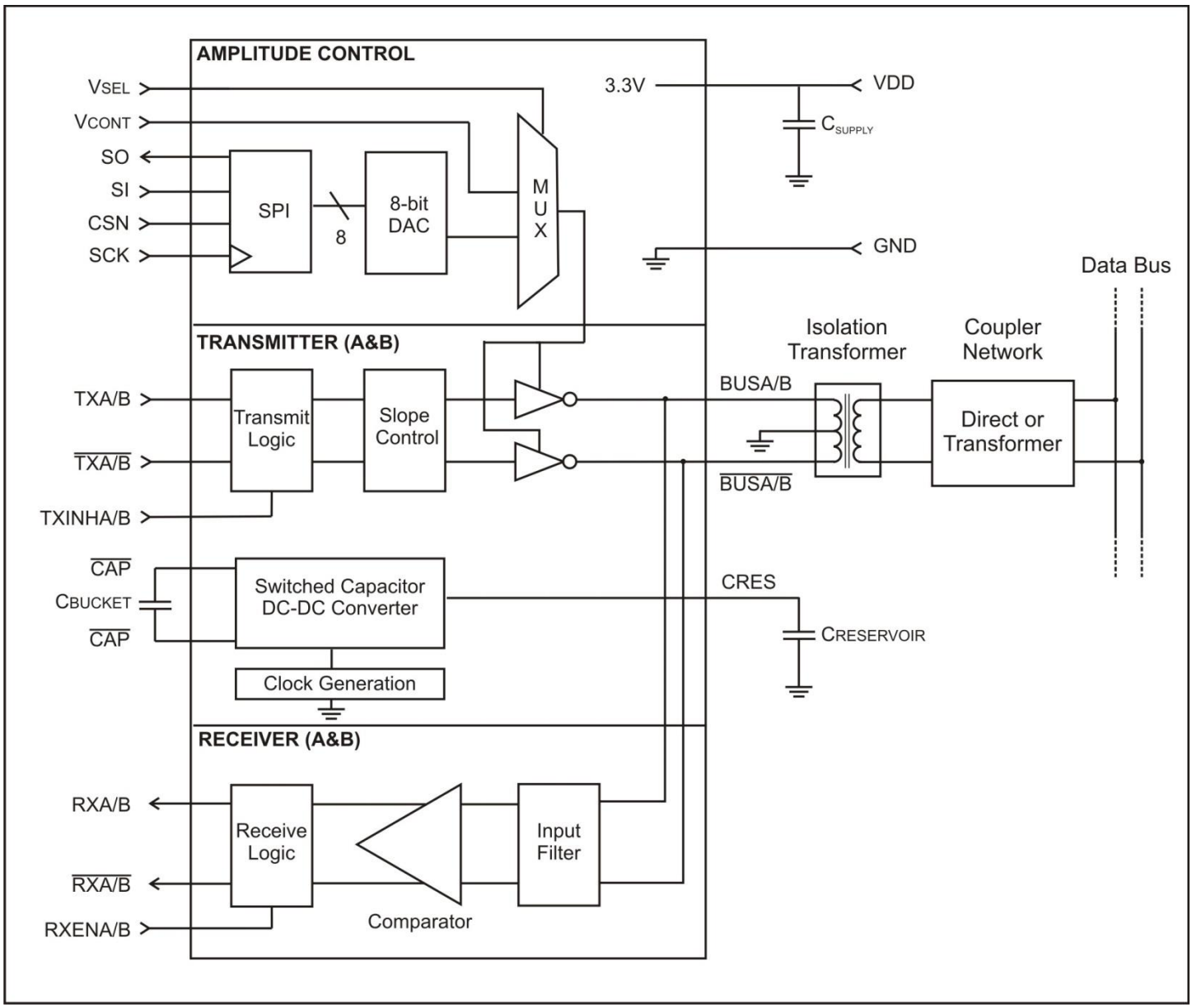


44 Pin Plastic 7mm x 7mm Chip-scale package



28 – Pin Ceramic Side-Brazed DIP

BLOCK DIAGRAM



PIN DESCRIPTIONS

PIN	SYMBOL	FUNCTION	DESCRIPTION
1	VCONT	Analog input	Transmit output amplitude control (0-3.3 Vdc, see Figure 8)
2	BUSA	Analog output	MIL-STD-1553 bus driver A, positive signal
3	$\overline{\text{BUSA}}$	Analog output	MIL-STD-1553 bus driver A, negative signal
4	RXENA	Digital input	Receiver A enable. If low, forces RXA and $\overline{\text{RXA}}$ low
5	GND	Power supply	Ground for bus A and bus B
6	VDD	Power supply	+3.3 volt power for both bus A and bus B
7	BUSB	Analog output	MIL-STD-1553 bus driver B, positive signal
8	$\overline{\text{BUSB}}$	Analog output	MIL-STD-1553 bus driver B, negative signal
9	VDD	Power supply	+3.3 volt power for both bus A and bus B
10	$\overline{\text{CAP}}$	Analog	Negative connection for external capacitor C_{BUCKET}. See Table 5 for recommended capacitor type.
11	CAP	Analog	Positive connection for external capacitor C_{BUCKET}. See Table 5 for recommended capacitor type.
12	CRES	Analog	Positive connection for external capacitor $C_{RESERVOIR}$. See Table 5 for recommended capacitor type.
13	RXENB	Digital input	Receiver B enable. If low, forces RXB and $\overline{\text{RXB}}$ low
14	$\overline{\text{RXB}}$	Digital output	Receiver B output, inverted
15	RXB	Digital output	Receiver B output, non-inverted
16	VSEL	Digital input	SPI enable. Tri-level inputs. If low, forces DAC value to control the output amplitude with 0-4.9V range in 19mV step size. If floating, forces VCONT A/B to control output amplitude. If high, forces DAC value to control the output amplitude with 0-26V range in 101mV step size
17	TXINHB	Digital input	Transmit inhibit, bus B. If high BUSB, $\overline{\text{BUSB}}$ disabled
18	TXB	Digital input	Transmitter B digital data input, non-inverted
19	$\overline{\text{TXB}}$	Digital input	Transmitter B digital data input, inverted
20	$\overline{\text{RXA}}$	Digital output	Receiver A output, inverted
21	RXA	Digital output	Receiver A output, non-inverted
22	TXINHA	Digital input	Transmit inhibit, bus A. If high BUSA, $\overline{\text{BUSA}}$ disabled
23	SCK	Digital input	SPI Clock
24	CSN	Digital input	SPI Chip Select, Active Low, internal 30KΩ pull-up
25	SO	Digital output	SPI serial data output
26	SI	Digital input	SPI serial data input, internal 30KΩ pull-up
27	TXA	Digital input	Transmitter A digital data input, non-inverted
28	$\overline{\text{TXA}}$	Digital input	Transmitter A digital data input, inverted

FUNCTIONAL DESCRIPTION

The HI-1590 data bus transceiver contains differential voltage source drivers and differential receivers. They are intended for applications using a MIL-STD-1553 A/B data bus. The device produces a trapezoidal output waveform during transmission.

TRANSMITTER

Data input to the device's transmitter section is from the complementary CMOS / TTL inputs TXA/B and $\overline{\text{TXA/B}}$. The transmitter accepts Manchester II bi-phase data and converts it to differential voltages on BUSA/B and $\overline{\text{BUSA/B}}$. The transceiver outputs are either direct or transformer coupled to the MIL-STD-1553 data bus. Both coupling methods produce a nominal voltage on the bus of 7.5 volts peak to peak at VCONT = 3.3 Vdc or maximum 8-bit DAC value 255. Refer to Figure 8 and Figure 9 for transmitter output amplitudes at other values of DAC or VCONT between 0 – 3.3 Vdc.

The transmitter is automatically inhibited and placed in the high impedance state when both TXA/B and $\overline{\text{TXA/B}}$ are either at a logic "1" or logic "0" simultaneously. A logic "1" applied to the TXINHA/B input will force the transmitter to the high impedance state, regardless of the state of TXA/B and $\overline{\text{TXA/B}}$.

DAC (Digital-to-Analog Converter) and VCONT

The 8 bits written into the SPI register are the input to the DAC. This DAC can control the amplitude of the HI-1590 transmitter output voltage by pulling VSEL high or low according to the following table:

VSEL	Control Source	Output Amplitude Range @ Point A_T	Step Size (mV)
High	8-bit DAC via SPI	0 - 26V	101mV
Float	V_{CONT} analog via pin 1	0 - 26V	Analog
Low	8-bit DAC via SPI	0 – 4.90V	19mV

When pulling VSEL high, the output amplitude (measured at Point "A_T" in Figure 7) ranges between 0 – 26 Volts in ~101mV steps as described by the following equation:

Y = 0.101x **(Equation 1)**

Where Y is the output amplitude Vo and x = DAC values $0 \le x \le 255$. Figure 9 plots this relationship between the DAC value input and the output voltage amplitude.

When pulling VSEL low, the output amplitude (measured at Point "A_T" in Figure 7) ranges between 0 – 4.90 Volts in ~19mV steps as described by the following equation:

Y = 0.019x **(Equation 2)**

Where Y is the output amplitude Vo, and x = DAC values $0 \le x \le 255$). Figure 10 plots this relationship between the DAC value input and the output voltage amplitude.

RECEIVER

The receiver accepts bi-phase differential data from the MIL-STD-1553 bus through the same direct or transformer coupled interface as the transmitter. The receiver's differential input stage drives a filter and threshold comparator that produces CMOS/TTL data at the RXA/B and $\overline{\text{RXA/B}}$ output pins.

Each set of receiver outputs can be independently forced to a logic "0" by setting RXENA or RXENB low.

MIL-STD-1553 BUS INTERFACE

A direct coupled interface (see Figure 4) uses a 1:2.5 ratio isolation transformer and two 55 Ω isolation resistors between the transformer and the bus.

In a transformer coupled interface (see Figure 4), the transceiver is also connected to a 1:1.25 isolation transformer which in turn is connected to a 1:1.4 coupling transformer. The transformer coupled method also requires two coupling resistors equal to 75% of the bus characteristic impedance (Zo) between the coupling transformer and the bus.

SERIAL PERIPHERAL INTERFACE (SPI) BASICS

The HI-1590 uses an SPI synchronous serial interface for host access to the internal DAC register. Host serial communication is enabled through the Chip Select CSN pin, and is accessed via a three-wire interface consisting of Serial Data Input (SI) from the host, Serial Data output (SO) to the host and Serial Clock (SCK). All read/write cycles are completely self-timed.

The SPI (Serial Peripheral Interface) protocol specifies master and slave operation; the HI-1590 operates as an SPI slave.

The SPI protocol defines two parameters, CPOL (clock polarity) and CPHA (clock phase). The possible CPOL-CPHA combinations define four possible "SPI Modes". Without describing details of the SPI modes, the HI-1590 operates in

mode 0 where input data for each device (master and slave) is clocked on the rising edge of SCK, and output data for each device changes on the falling edge (CPHA = 0, CPOL = 0). Be sure to set the host SPI logic for mode 0.

As seen in Figure 1, SPI Mode 0 holds SCK in the low state when idle.

The SPI protocol transfers serial data as 8-bit bytes. Once CSN chip select is asserted, the next 8 rising edges on SCK latch input data into the master and slave devices, starting with each byte's most-significant bit. The HI-1590 SPI can be clocked at up to 20MHz.

HI-1590 SPI COMMANDS

For the HI-1590, each SPI operation is both a read and a simultaneous write. When a host transfers an 8 bit DAC setting, the current byte in the shift register is shifted out and read at the SO pin as the new byte is shifted into the register simultaneously as shown in Figure 1. The newly arrived byte is transferred from the host to the device on the rising edge of CSN.

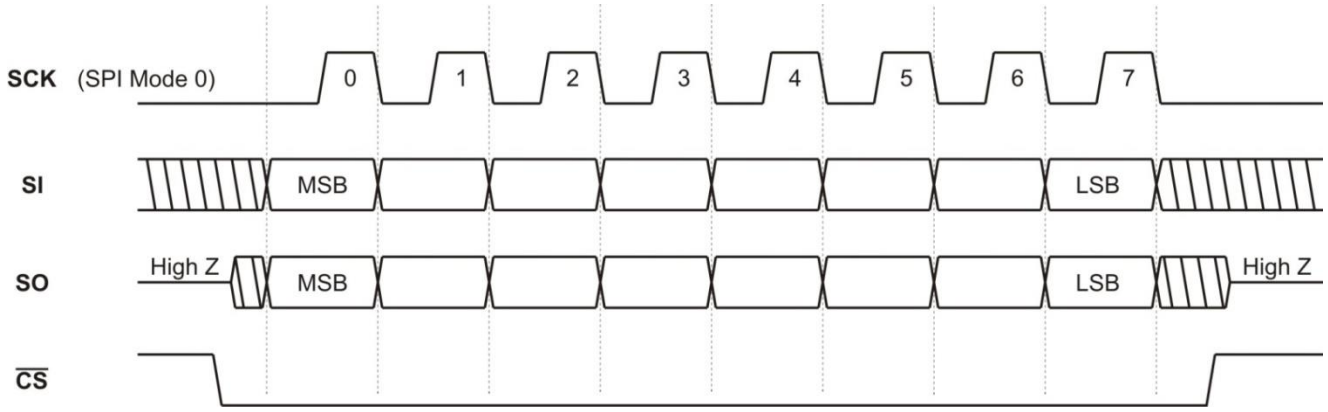


Figure 1: Single-Byte Transfer using SPI Protocol Mode 0

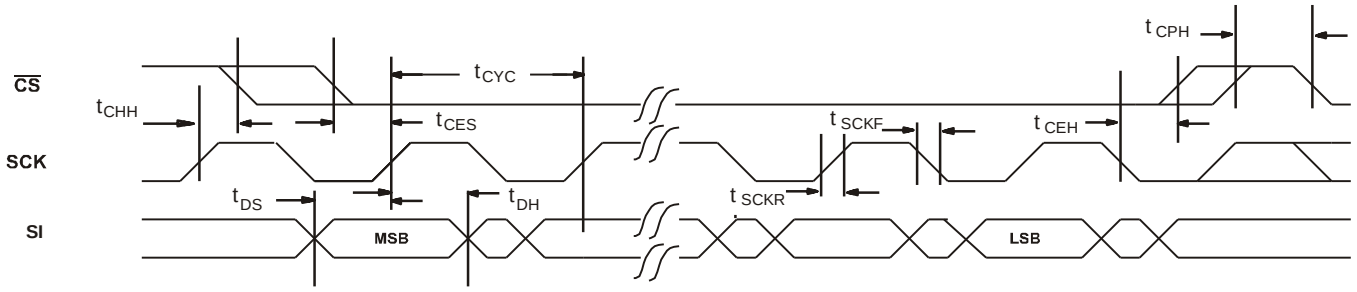


Figure 2: SPI Serial Input Timing

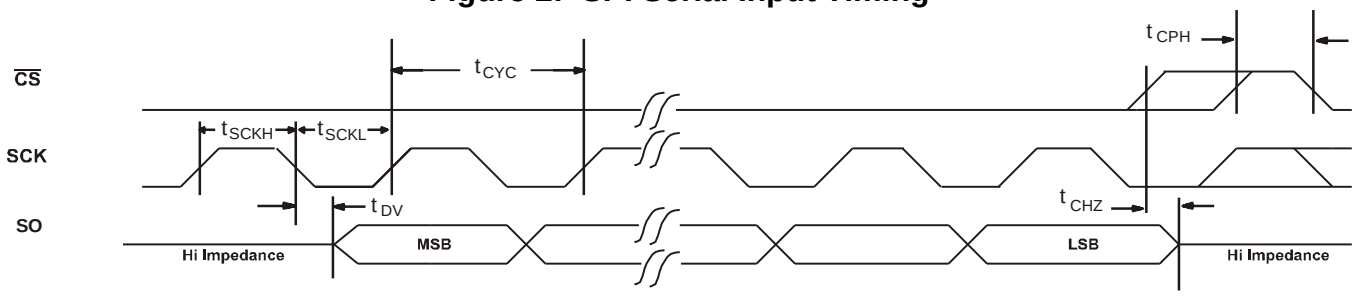


Figure 3: SPI Serial Output Timing

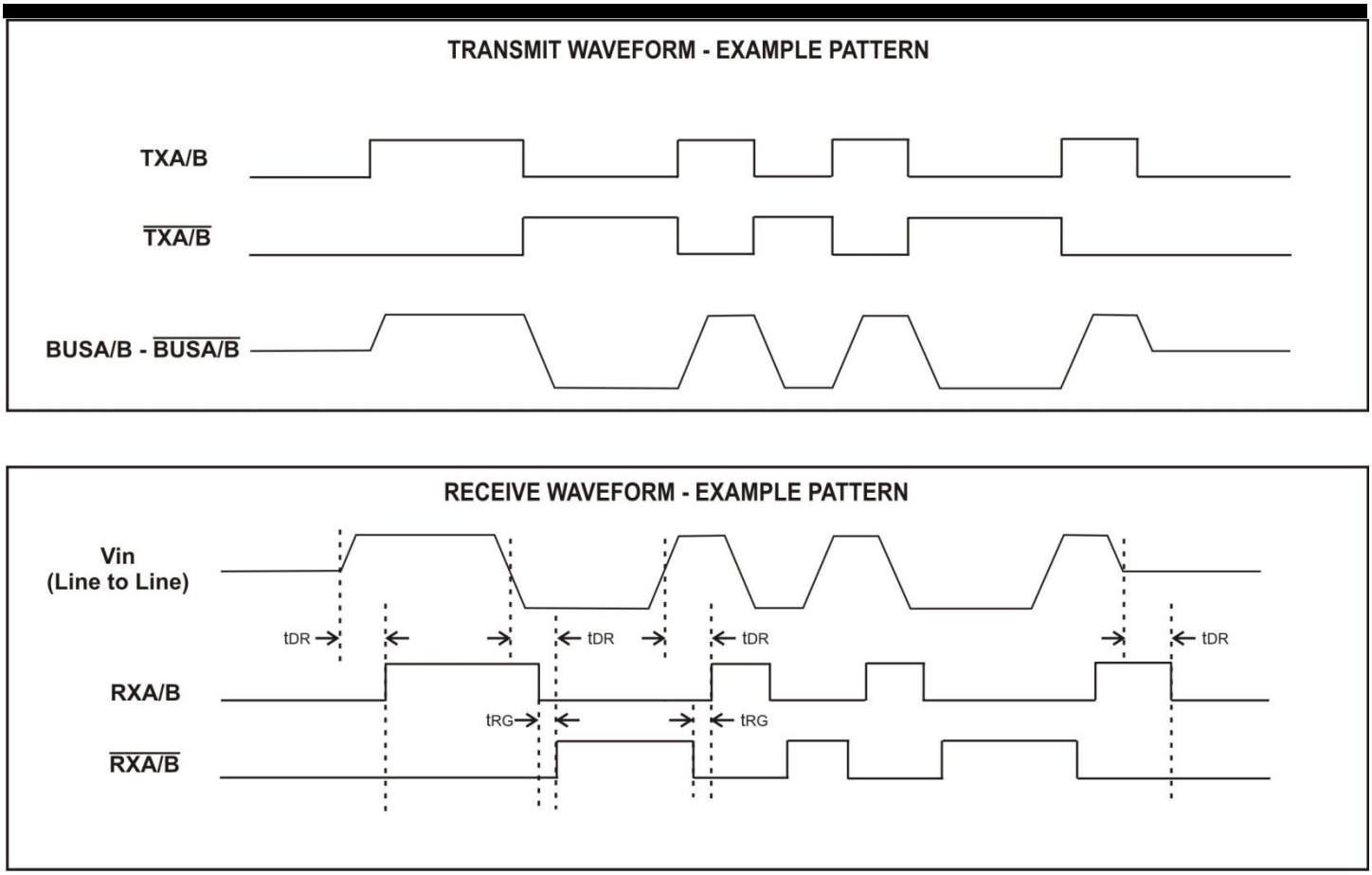


Figure 4: Transmit and Receive Waveforms

ABSOLUTE MAXIMUM RATINGS

Supply voltage (V_{DD})	-0.3 V to +5 V
Logic input voltage range	-0.3 V DC to +3.6V
Voltage at BUSA/B or $\overline{BUSA/B}$ pins	+/- 7 V
Driver peak output current	+1.0 A
Solder Reflow Temperature	260°C
Junction Temperature	175°C
Storage Temperature	-65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltage

V_{DD} ……..……..3.3V….±5%

Temperature Range

Industrial ……..……...-40°C to +85°C
Extended……..……-55°C to +125°C

NOTE: Stresses above absolute maximum ratings or outside recommended operating conditions may cause permanent damage to the device. These are stress ratings only. Operation at the limits is not recommended.

Table 1. DC ELECTRICAL CHARACTERISTICS

V_{DD} = 3.3V, GND = 0V, VCONT = 3.3V, TA = Operating Temperature Range (unless otherwise specified).

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Operating Voltage	V_{DD}		3.15	3.3	3.45	V
Total Supply Current	I_{CC1}	Not Transmitting		25	40	mA
	$I_{CC\ 2}$	Transmit one bus @ 50%duty cycle		225	320	mA
	$I_{CC\ 3}$	Transmit one bus @ 100% duty cycle		750	900	mA
Power Dissipation	PD_1	Not transmitting			0.06	W
	PD_2	Transmit one bus @ 100% duty cycle		0.5	1.0	W
Min. Input Voltage (HI)	V_{IH}	Digital inputs	70%			V_{DD}
Max. Input Voltage (LO)	V_{IL}	Digital inputs			30%	V_{DD}
Min. Input Current (HI)	I_{IH}	Digital inputs			20	uA
Max. Input Current (LO)	I_{IL}	Digital inputs	-20			uA
Min. Output Voltage (HI)	V_{OH}	I_{OUT} = -1.0mA, Digital outputs	90%			V_{DD}
Max. Output Voltage (LO)	V_{OL}	I_{OUT} = 1.0mA, Digital outputs			10%	V_{DD}
RECEIVER (Measured at Point "A_D" in Figure 6 unless otherwise specified)						
Input resistance	R_{IN}	Differential (at chip BUS pins)	2			kΩ
Input capacitance	C_{IN}				5	pF
Common mode rejection ratio	CMRR		40			dB
Input common mode voltage	V_{ICM}		-10.0		10.0	V-pk
Threshold Voltage – Direct-coupled Detect	V_{THD}	1 MHz Sine Wave (Measured at Point "A_D" in Figure 6) (RX pulse width 70ns)	1.15			V_{p-p}
No Detect	V_{THND}	No pulse at RXA/B, $\overline{RXA/B}$			0.28	V_{p-p}
Threshold Voltage – Transformer-coupled Detect	V_{THD}	1 MHz Sine Wave (Measured at Point "A_T" in Figure 7) (RX pulse width 70ns)	0.86			V_{p-p}
No Detect	V_{THND}	No pulse at RXA/B, $\overline{RXA/B}$			0.20	V_{p-p}

Table 2. DC ELECTRICAL CHARACTERISTICS (cont.)

VDD = 3.3V, GND = 0V, VCONT = 3.3V, TA = Operating Temperature Range (unless otherwise specified).

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
TRANSMITTER (Measured at Point "A_D" in Figure 6 unless otherwise specified)						
Maximum Output Voltage Direct coupled	V_{OUT}	35 Ω load (Measured at Point "A_D" in Figure 6)	6.1		9.0	V_{p-p}
Transformer coupled	V_{OUT}	70 Ω load (Measured at Point "A_T" in Figure 7)	20.0		28.0	V_{p-p}
Output Noise	V_{ON}	Differential, inhibited			10	mV_{p-p}
Output Dynamic Offset Voltage Direct coupled	V_{DYN}	35 Ω load (Measured at Point "A_D" in Figure 6)	-90		90	mV
Transformer coupled	V_{DYN}	70 Ω load (Measured at Point "A_T" in Figure 7)	-250		250	mV
Output resistance	R_{OUT}	Differential, not transmitting	10			kΩ
Output Capacitance	C_{OUT}	1 MHz sine wave			15	pF
Control Line Resistance	R_{CONT}			5		kΩ
DAC Deviation from programmed value	DAC_{dev}		-3		+3	bits

Table 3. AC ELECTRICAL CHARACTERISTICS

VDD = 3.3V, GND = 0V, TA = Operating Temperature Range (unless otherwise specified).

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
RECEIVER (Measured at Point "A_T" in Figure 6)						
Receiver Delay	t_{DR}	From input zero crossing to RXA/B or $\overline{RXA/B}$			450	ns
Receiver gap time	t_{RG}	Spacing between RXA/B and $\overline{RXA/B}$ pulses 1 MHz sine wave applied at point "AT" Figure 6, amplitude range 0.86 Vp-p to 27.0Vp-p	90		365	ns
Receiver Enable Delay	t_{REN}	From RXENA/B rising or falling edge to RXA/B or $\overline{RXA/B}$			40	ns
TRANSMITTER (Measured at Point "A_D" in Figure 6)						
Driver Delay	t_{DT}	TXA/B, $\overline{TXA/B}$ to BUSA/B, $\overline{BUSA/B}$			150	ns
Rise time	t_r	35 Ω load	100		300	ns
Fall time	t_f	35 Ω load	100		300	ns
Inhibit Delay	t_{dI-H}	Inhibited output			100	ns
	t_{DI-L}	Active output			150	ns
DAC Settling Time	t_{DAC}			50		ms

Table 4. AC ELECTRICAL CHARACTERISTICS (cont.)

VDD = 3.3V, GND = 0V, TA = Operating Temperature Range (unless otherwise specified).

SPI INTERFACE TIMING (See Figure 2 & Figure 3)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
SCK clock period	t_{CYC}	50			ns
CS active after last SCK rising edge	t_{CHH}	5			ns
CS setup time to first SCK rising edge	t_{CES}	5			ns
CS hold time after last SCK falling edge	t_{CEH}	5			ns
CS inactive between SPI instructions	t_{CPH}	55			ns
SPI SI Data set-up time to SCK rising edge	t_{DS}	10			ns
SPI SI Data hold time after SCK rising edge	t_{DH}	10			ns
SCK rise time	t_{SCKR}			10	ns
SCK fall time	t_{SCKF}			10	ns
SCK pulse width high	t_{SCKH}	20			ns
SCK pulse width low	t_{SCKL}	20			ns
SO valid after SCK falling edge	t_{DV}			20	ns
SO high-impedance after CS inactive	t_{CHZ}			20	ns

Table 5. DC-DC CONVERTER CHARACTERISTICS

VDD = 3.3V, GND = 0V, TA = Operating Temperature Range (unless otherwise specified).

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Start-up transient	T_{start}		-	-	10	ms
Operating Switching Frequency	f_{SW}			550		kHz
Recommended Capacitors: X7R dielectric, low ESR, 200m Ω max. Rated voltage: ≥10V Material: Ceramic or Tantalum, preferably multilayer.	C_{BUCKET} $C_{RESERVOIR}$	$C_{RESERVOIR}$ / C_{BUCKET} ≥ 10	2.2 22	4.7 47	- -	µF µF
Recommended Capacitor: Rated voltage: ≥6.3V Material Tantalum	C_{SUPPLY}	C_{SUPPLY} ≥ $C_{RESERVOIR}$ (connect from VDD to GND)	47	68	-	µF

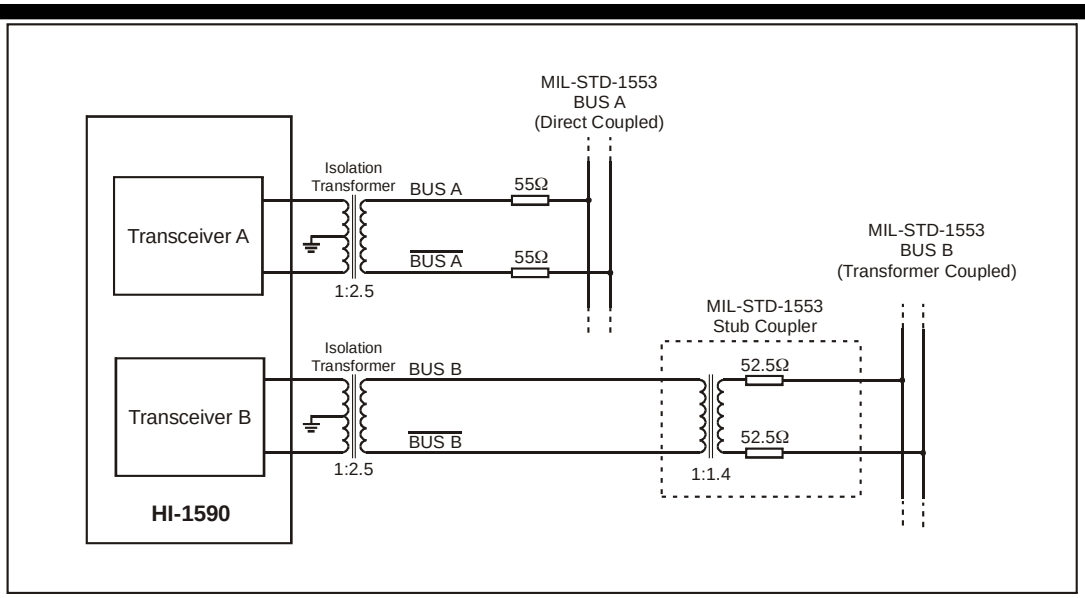


Figure 5: Bus Connection Example

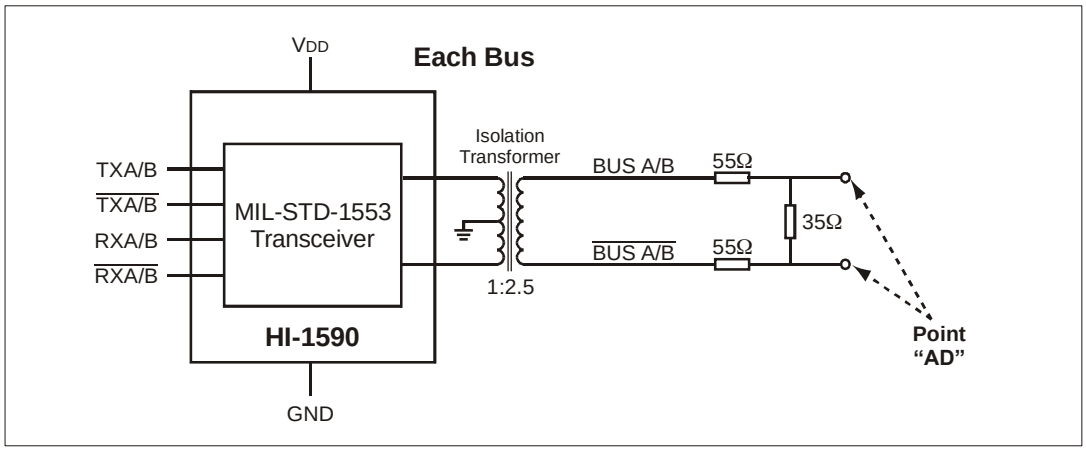


Figure 6: Direct Coupled Test Circuit

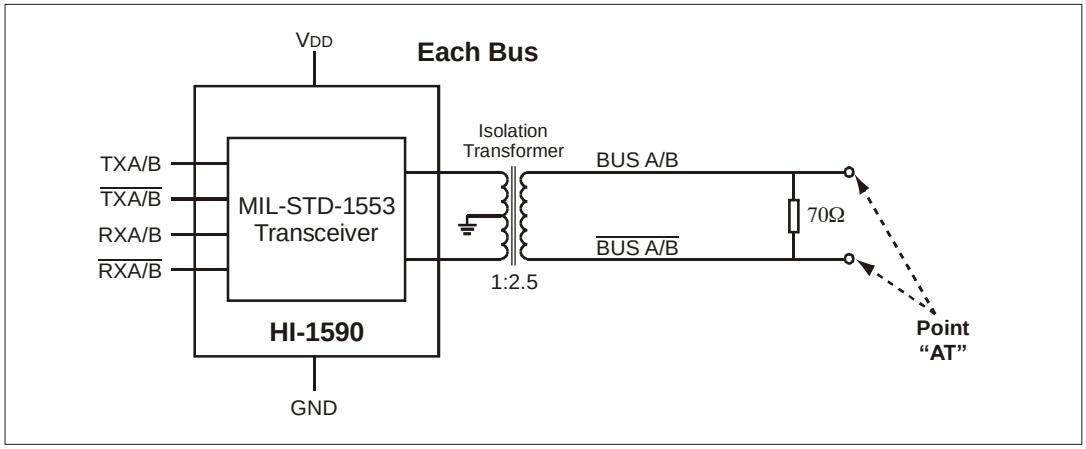


Figure 7: Transformer Coupled Test Circuit

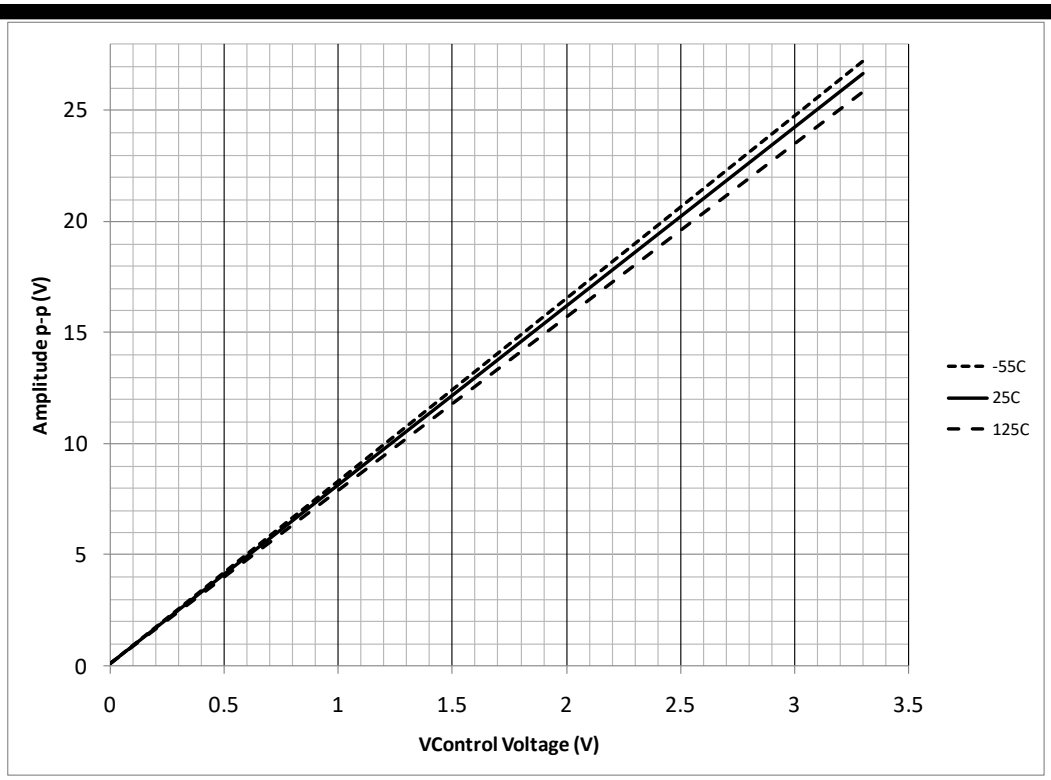


Figure 8: VSEL Float - Transmitter Output Amplitude (Vo) vs. VCONT Voltage ("AT", Figure 6)

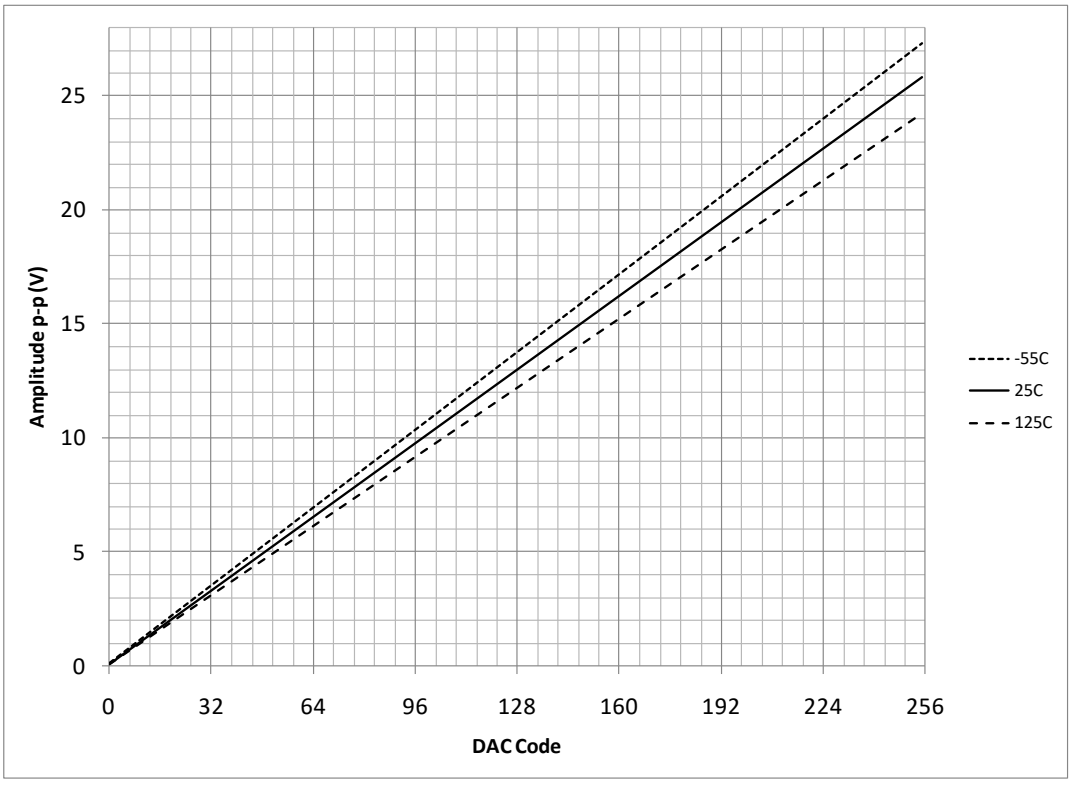


Figure 9: VSEL High - Transmitter Output Amplitude (Vo) vs. DAC value ("AT", Figure 6)

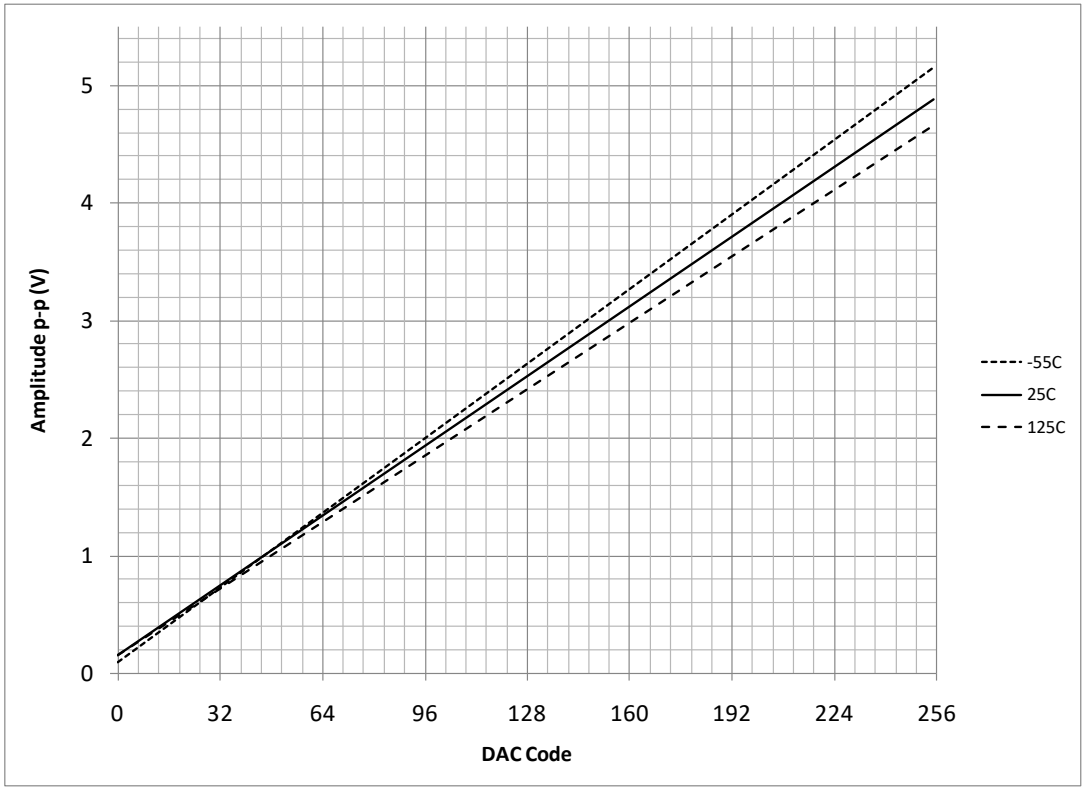


Figure 10: VSEL Low - Transmitter Output Amplitude (Vo) vs. DAC value ("AT", Figure 6)

APPLICATIONS NOTE

Holt Applications Note AN-500 provides circuit design notes regarding the use of Holt's family of MIL-STD-1553 transceivers. Layout considerations, as well as recommended interface and protection components are included.

DAISY CHAIN CONFIGURATION

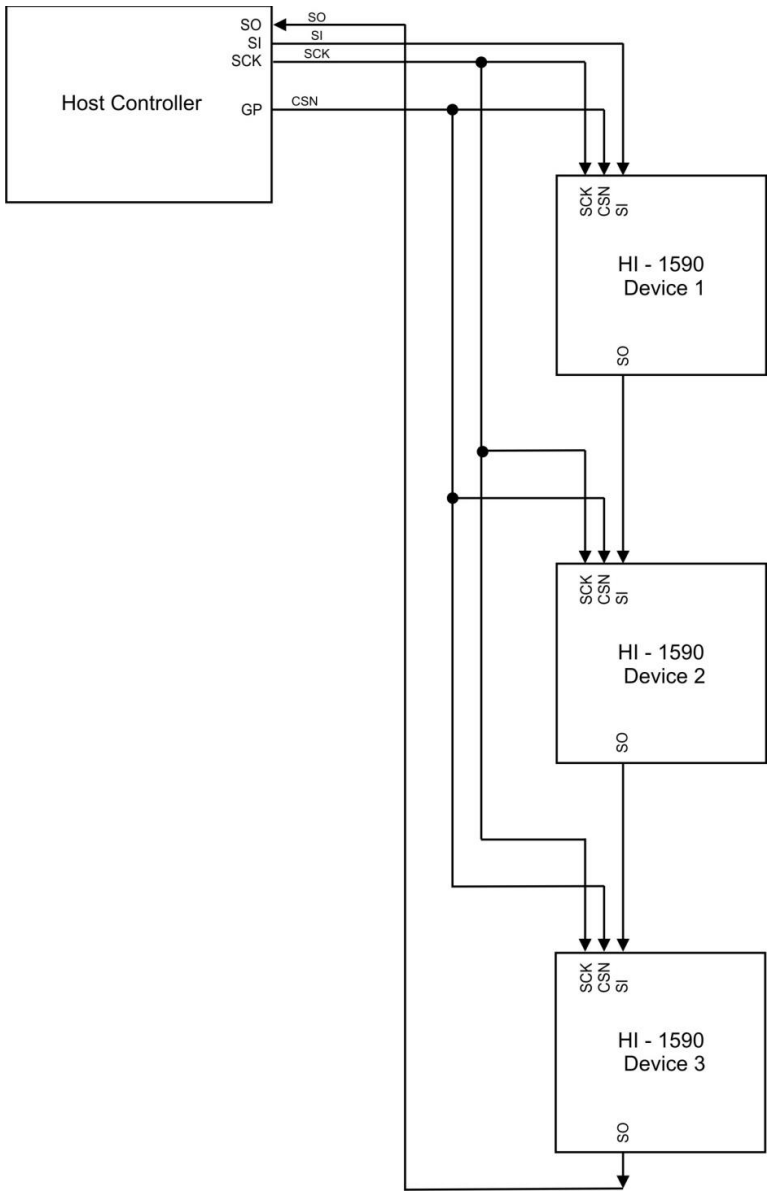


Figure 11: Daisy Chain Configuration

When using the SPI daisy chain configuration shown in Figure 11, the SPI waveform illustrated in Figure 12 should be used. Each SPI byte needs to be preceded by a falling /CS signal, and followed by a rising /CS signal. Also, the first byte sent will set the amplitude for the last device in the SPI chain, and the last byte sent will set the amplitude for the first device in the chain. As each byte is sent, the amplitude will change. In this example, the amplitude of each of the devices will change 3 times. The amplitude should be set before transmitting the data.

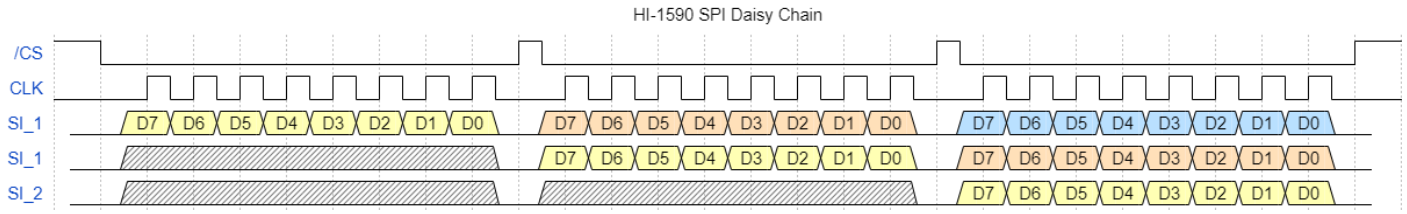


Figure 12: Example Daisy Chain Waveform and Required /CS Sequence

Table 6. RECOMMENDED TRANSFORMERS

The HI-1590 transceiver has been characterized for compliance with the electrical requirements of MIL-STD-1553 when used with the following transformers. Holt recommends Premier Magnetics parts as offering the best combination of electrical performance, low cost and small footprint.

MANUFACTURER	PART NUMBER	APPLICATION	TURNS RATIO(S)	DIMENSIONS
Premier Magnetics	PM-DB2702(+)[1]	Stub coupling	1:1.4	.625 x .625 x .250 inches
Premier Magnetics	PM-DB2776(+)[2]	Isolation	Dual ratio 1:2.5	0.675 x 0.4 x 0.185 inches
Premier Magnetics	PM-DB2762(+)[3]	Isolation	Dual ratio 1:2.5	0.4 x 0.4 x 0.330 inches

Note 1: Parts with "+" following part number are RoHS compliant.
Note 2: Dual side-by-side transformers for low profile.
Note 3: Dual stacked transformers for small footprint.

ORDERING INFORMATION

HI-1590PC x x (Plastic)

PART NUMBER	LEAD FINISH
Blank	NiPdAu
F	NiPdAu (Pb-free, RoHS compliant)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C to +85°C	I	NO
T	-55°C to +125°C	T	NO

PART NUMBER	RXENA=0		RXENB=0		PACKAGE DESCRIPTION
	RXA	RXA	RXB	RXB	
1590PC	0	0	0	0	44 PIN PLASTIC CHIP-SCALE QFN with optional SPI controlled DAC

HI-1590CD x (Ceramic)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN	LEAD FINISH
I	-40°C to +85°C	I	NO	Gold (Pb-free, RoHS compliant)
T	-55°C to +125°C	T	NO	Gold (Pb-free, RoHS compliant)
M	-55°C to +125°C	M	YES	Tin/Lead (Sn / Pb) Solder

PART NUMBER	RXENA=0		RXENB=0		PACKAGE DESCRIPTION
	RXA	RXA	RXB	RXB	
1590CD	0	0	0	0	28 PIN CERAMIC SIDE BRAZED DIP (28C) with optional SPI controlled DAC

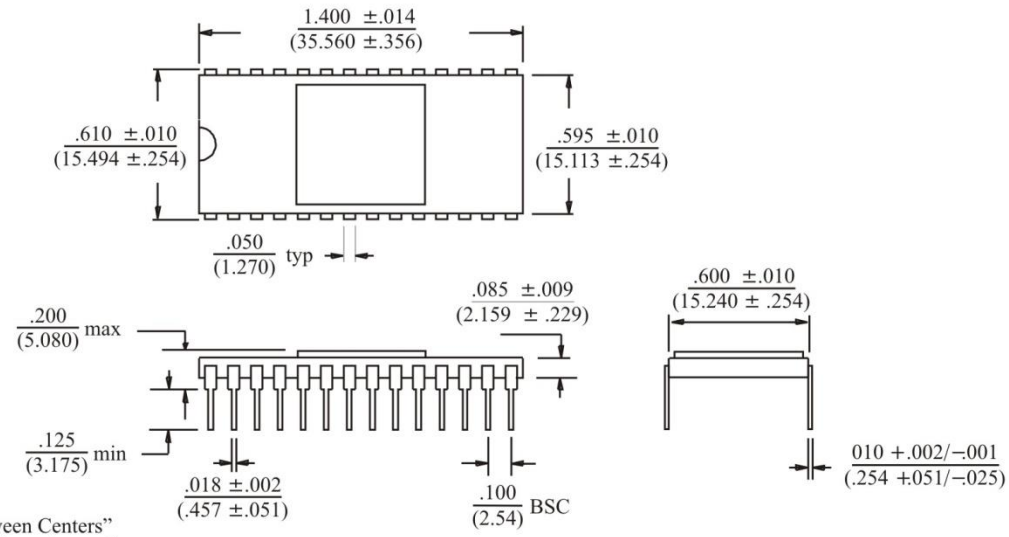
REVISION HISTORY

Document	Rev.	Date	Description of Change
DS1590	NEW	10/16/2014	Initial Release.
	A	11/12/2014	Add SPI timing information to AC characteristics. Update SPI Timing Diagram.
	B	01/22/2015	Remove max power dissipation from Maximum Ratings. Remove reference to ESOIC package. Update Recommended Transformers.
	C	11/22/2017	Correct error in Fig. 3. SO is high impedance after CS inactive, not SCK falling edge. Correct typos in Table 1. Correct error in Figure 5. Remove Thermal Characteristics Table (see website for thermal resistance data).
	D	02/13/2018	Add Absolute Maximum Rating for voltage at BUS pins.
	E	09/01/2020	Update QFN package lead finish to NiPdAu.
	F	12/16/2021	Clarify how to configure the device for daisy chain operation.

28-PIN CERAMIC SIDE-BRAZED DIP

inches (millimeters)

Package Type: 28C

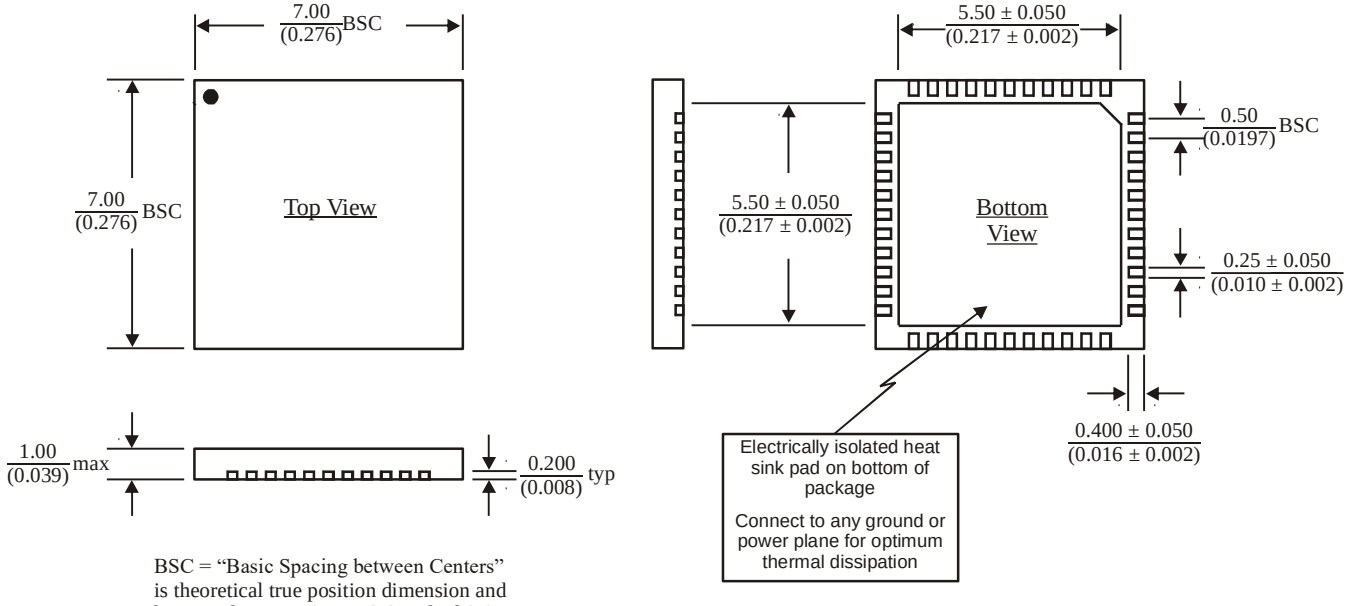


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

44-PIN PLASTIC CHIP-SCALE PACKAGE (QFN)

millimeters (inches)

Package Type: 44PCS



BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)